Claims

What is claimed is:

1. A power amplifier circuit comprising:

an input port for receiving a RF input signal;

an output port for providing therefrom a RF output signal, the RF output signal being an amplified version of the RF input signal;

a supply voltage input port for receiving a supply voltage;

a voltage regulator circuit for receiving the supply voltage and for providing a regulated supply voltage;

a first amplification stage having a first gain and for receiving one of a signal derived from the RF input signal and the RF input signal and for providing a first amplified RF signal, the first amplification stage coupled to the voltage regulator circuit for receiving the regulated supply voltage; and,

a second amplification stage having a second gain and coupled to the first amplification stage for receiving one of a signal derived from the first amplified RF signal and the first amplified RF signal and coupled to the output port for providing the output signal thereto, the second amplification stage coupled to the supply voltage input port for receiving the supply voltage other than regulated by the voltage regulator circuit.

2. A power amplifier circuit according to claim 1, comprising a control port coupled to the voltage regulator circuit and for receiving a control signal for controlling the regulated supply voltage.

3. A power amplifier circuit according to claim 1, comprising a control port coupled to the first amplification stage and for receiving a control signal for controlling the first gain of the first amplification stage.

4. A power amplifier circuit according to claim 1, comprising a control port coupled to the second amplification stage and for receiving a control signal for controlling a second gain of the second amplification stage.

5. A power amplifier circuit according to claim 1, comprising a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit, the temperature signal for provision to at least two of the regulator circuit and the first amplification stage and the second amplification stage.

6. A power amplifier circuit according to claim 5, wherein the temperature sensing circuit is integrated on a same die as the power amplifier circuit.

7. A power amplifier circuit according to claim 1, comprising a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit, the temperature signal for provision to the regulator circuit.

8. A power amplifier circuit according to claim 1, comprising a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit, the temperature signal for provision to the first amplification stage.

9. A power amplifier circuit according to claim 1, comprising a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit, the temperature signal for provision to the second amplification stage.

10. A power amplifier circuit according to claim 1, comprising a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense signal in dependence thereon, the sense signal for provision to the regulator circuit.

11. A power amplifier circuit according to claim 10, comprising a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense

signal in dependence thereon, the sense signal for provision to at least one of the first amplification stage and the second amplification stage.

12. A power amplifier circuit according to claim 1, comprising a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense signal in dependence thereon, the sense signal for provision to the first amplification stage.

13. A power amplifier circuit according to claim 1, comprising a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense signal in dependence thereon, the sense signal for provision to the second amplification stage.

14. A power amplifier circuit according to claim 11, wherein the voltage sensing circuit is integrated on a same die as the power amplifier circuit.

15. A power amplifier circuit according to claim 2, wherein the voltage regulator circuit comprises a FET having one of the drain and source terminals coupled to the supply voltage input port for receiving the supply voltage and the other of the drain and source terminals coupled to the first amplification stage for providing the regulated supply voltage.

16. A power amplifier circuit according to claim 15, wherein the voltage regulator circuit comprises an operational amplifier circuit, the operational amplifier circuit having a first input port, a second input port and an output port, the first input port thereof coupled to the control port for receiving the control signal and the output port thereof coupled to a gate terminal of the FET.

17. A power amplifier circuit according to claim 16, comprising:

a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit;

a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense signal in dependence thereon; and,

a first summing circuit having an output port, a first input port, a second input port and a third input port, the output port thereof coupled to the second input port of the operational amplifier circuit, the first input port thereof coupled to one of the drain and source terminals of the FET for receiving the regulated supply voltage, the second input port thereof coupled to the voltage sensing circuit for receiving the sense signal, and the third input port thereof coupled to the temperature sensing circuit for receiving the temperature signal therefrom.

18. A power amplifier circuit according to claim 16, comprising a feedback sense circuit disposed between one of the drain and source terminals of the FET and the second input port of the operational amplifier circuit, the feedback sense circuit for sensing of the regulated supply voltage from the FET.

19. A power amplifier circuit according to claim 18, wherein the feedback sense circuit comprises a voltage divider circuit.

20. A power amplifier circuit according to claim 18, wherein the feedback sense circuit comprises an amplitude shifting circuit.

21. A power amplifier circuit according to claim 18, wherein the feedback sense circuit is integrated on a same die as the power amplifier circuit.

22. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to at least one of the first amplification stage and the second amplification stage.

23. A power amplifier circuit according to claim 22, wherein the detector circuit is integrated on a same die as the power amplifier circuit.

24. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to the first amplification stage.

25. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal to the second amplification stage.

26. A power amplifier circuit according to claim 1, comprising a detector circuit having an input port coupled to the power amplifier circuit output port for determining a RF output signal power level and having an output port for providing an output level signal.

27. A power amplifier circuit according to claim 22, wherein the detector circuit comprises at least a difference amplifier circuit having a first input port, a second input port and an output port, the first input port coupled to the detector circuit input port and the second input port for receiving a current mirrored from the RF output signal current.

28. A power amplifier circuit according to claim 27, wherein the detector circuit comprises a second summing circuit having at least two input ports and an output port, the at least two input ports thereof coupled to the output port of the at least a difference amplifier circuit, the output port thereof coupled to at least one of the first amplification stage and the second amplification stage.

29. A power amplifier circuit according to claim 28, wherein the detector circuit comprises:

at least a sense transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the second input port of the at least a difference amplifier circuit;

at least a sense resistor disposed in parallel with the first and second input ports of the at least a difference amplifier circuit; and,

a mirror transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the input port of the detector circuit, the base terminal of the current mirror transistor is coupled to the base terminal of the at least a sense transistor, where the mirror transistor is for current mirroring RF output signal current.

30. A power amplifier circuit according to claim 1, wherein each amplification stage comprises at least a transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals coupled to one of the supply voltage and regulated supply voltage and the other one of the emitter and collector terminals coupled to ground.

31. A power amplifier circuit according to claim 30, wherein each amplification stage comprises at least a current source coupled to the base terminal of the at least a transistor.

32. A power amplifier circuit according to claim 31, wherein the at least a current source is integrated on a same die as the power amplifier circuit.

33. A power amplifier circuit according to claim 1, wherein each amplification stage comprises at least a transistor having a drain terminal, a source terminal and a gate terminal, one of the source and drain terminals coupled to one of the supply voltage and

regulated supply voltage and the other one of the source and drain terminals coupled to ground.

34. A power amplifier circuit according to claim 33, wherein each amplification stage comprises at least a voltage source coupled to the gate terminal of the at least a transistor.

35. A power amplifier circuit according to claim 34, wherein the at least a voltage source is integrated on a same die as the power amplifier circuit.

36. A power amplifier circuit according to claim 1, comprising a capacitor disposed between the first amplification stage and the second amplification stage.

37. A power amplifier circuit according to claim 1, wherein the voltage regulator circuit and the first amplification stage and the second amplification stage are integrated on a same die.

38. A power amplifier circuit according to claim 1, wherein the voltage regulator circuit is other than integrated on a same die.

39. A power amplifier circuit according to claim 1, wherein the supply voltage provided to the die is regulated for the first amplification stage using the voltage regulator circuit but other than regulated for the second amplification stage.

40. A power amplifier circuit according to claim 1, wherein the first amplification stage and the second amplification stage are disposed on the same substrate.

41. A method of amplifying a RF input signal to form a RF output signal that is an amplified version of the RF input signal comprising the steps of:

receiving the RF input signal;

providing a first amplification stage having a first gain;

providing a second amplification stage having a second gain;

receiving a first supply voltage;

regulating the first supply voltage to provide a regulated supply voltage;

providing the regulated supply voltage to the first amplification stage;

providing the first supply voltage to the second amplification stage; and,

amplifying one of a signal derived from the received RF input signal and the received RF input signal using the first amplification stage having the first gain and the second amplification stage having the second gain to form the RF output signal.

42. A method according to claim 41, comprising the steps of:

receiving a control signal; and,

varying the regulated supply voltage in dependence upon the received control signal.

43. A method according to claim 41, comprising the steps of:

receiving a control signal; and,

varying the first gain of the first amplification stage in dependence upon the received control signal.

44. A method according to claim 41, comprising the steps of:

receiving a control signal; and,

varying the second gain of the second amplification stage in dependence upon the received control signal.

45. A method according to claim 41, comprising the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal; and,

varying the regulated supply voltage in dependence upon the temperature signal.

46. A method according to claim 41, comprising the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal; and,

varying the first gain of the first amplification stage in dependence upon the temperature signal.

47. A method according to claim 41, comprising the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal; and,

varying the second gain of the second amplification stage in dependence upon the temperature signal.

48. A method according to claim 41, comprising the steps of:

sensing a supply voltage potential to provide a sense signal; and,

varying the regulated supply voltage in dependence upon the sense signal.

49. A method according to claim 41, comprising the steps of:

sensing a supply voltage potential to provide a sense signal; and,

varying the first gain of the first amplification stage in dependence upon the sense signal.

50. A method according to claim 41, comprising the steps of:

sensing a supply voltage potential to provide a sense signal; and,

varying the second gain of the second amplification stage in dependence upon the sense signal.

51. A method according to claim 41, comprising the steps of:

providing of a regulator circuit;

providing a FET disposed within the regulator circuit;

receiving a supply voltage at one of the FET drain and source terminals; and,

providing the regulated supply voltage from the other of the drain and source terminals of the FET.

52. A method according to claim 41, comprising the steps of:

sensing a temperature of the power amplifier circuit to provide a temperature signal;

sensing a potential of the supply voltage to provide a sense signal;

sensing a potential of the regulated supply voltage;

summing the received portion of the regulated supply voltage and the sense signal and the temperature signal to form a summed signal; and,

varying the regulated supply voltage in dependence upon the summed signal.

53. A method according to claim 41, comprising the steps of:

detecting the RF output signal power level to provide an output level signal; and

providing the output level signal to the first amplification stage.

54. A method according to claim 53, comprising the step of varying the first gain of the first amplification stage in dependence upon the output level signal.

55. A method according to claim 53, wherein the step of detecting comprises the steps of:

current mirroring the RF output signal current to form a RF output signal mirror current; and,

logarithmically amplifying the RF output signal mirror current to provide the output level signal to the first amplification stage.

56. A method according to claim 41, comprising:

detecting the RF output signal power level to provide an output level signal; and

providing the output level signal to the second amplification stage.

57. A method according to claim 56, comprising the step of varying the second gain of the second amplification stage in dependence upon the output level signal.

58. A method according to claim 56, wherein the step of detecting comprises the steps of:

current mirroring the RF output signal current to form a RF output signal mirror current; and,

logarithmically amplifying the RF output signal mirror current to provide the output level signal to the second amplification stage.

59. A method according to claim 56, wherein the step of detecting comprises the steps of:

detecting a first RF output signal power level to provide a first output level signal;

detecting a second RF output signal power level to provide a second output level signal;

summing the detected first output level signal and the detected second output level signal to form a summed signal; and,

providing the output level signal in dependence upon the summed signal.

60. A method according to claim 56, wherein the step of detecting comprises the steps of:

providing a first resistor having a first resistance;

detecting a first mirror current from the RF output current using the first resistance of the first resistor;

providing a second resistor having a second resistance;

detecting of a second mirror current from the RF output using the second resistance of the second resistor;

summing the detected first mirror current and the detected second mirror current to provide a summed signal; and,

forming the output level signal in dependence upon the summed signal.

61. A method according to claim 41, comprising the step of varying the first gain and the second gain to other than vary output power of the RF output signal.

62. A power amplifier circuit comprising:

an input port for receiving a RF input signal;

an output port for providing therefrom a RF output signal, the RF output signal being an amplified version of the RF input signal;

a supply voltage input port for receiving a supply voltage;

a voltage regulator circuit for receiving the supply voltage and for providing a regulated supply voltage;

a first amplification stage having a first gain for receiving one of a signal derived from the RF input signal and the RF input signal and for providing a first amplified RF signal, the first amplification stage coupled to the voltage regulator circuit for receiving the regulated supply voltage;

a second amplification stage having a second gain for receiving one of a signal derived from the first amplified RF signal and the first amplified RF signal and coupled to the output port for providing the output signal thereto, the second amplification stage coupled to the supply voltage input port for receiving the supply voltage, the supply voltage provided to the second amplification stage and other than regulated by the voltage regulator circuit;

a temperature sensing circuit disposed for sensing a temperature of the power amplifier circuit and for providing a temperature signal therefrom in dependence upon the sensed temperature of the power amplifier circuit, the temperature signal for provision to the regulator circuit and at least one of the first amplification stage and the second amplification stage;

a voltage sensing circuit disposed for sensing a potential of the supply voltage and for providing a sense signal in dependence thereon, the sense signal for provision to at least one of the regulator circuit and the first amplification stage and the second amplification stage; and,

a control port coupled to at least one of the voltage regulator circuit and the first amplification stage and the second amplification stage for at least one of respectively controlling the regulated supply voltage and the first gain and the second gain.

63. A power amplifier circuit according to claim 62, comprising:

a power output detector circuit having an input port coupled to the power amplifier circuit output port for detecting at least one of current and voltage from the RF

output signal and having an output port for providing a output level signal to at least one of the first amplification stage and the second amplification stage.

64. A power amplifier circuit according to claim 63, wherein the detector circuit comprises:

at least a sense transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the second input port of the at least a difference amplifier circuit;

at least a sense resistor disposed in parallel with the first and second input ports of the at least a difference amplifier circuit; and,

a mirror transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals thereof coupled to ground and the other one of the emitter and collector terminals coupled to the input port of the detector circuit, the base terminal of the current mirror transistor is coupled to the base terminal of the at least a sense transistor.

65. A power amplifier circuit according to claim 62, wherein the voltage regulator circuit comprises a FET having one of the drain and source terminals coupled to the supply voltage input port for receiving the supply voltage and the other of the drain and source terminals coupled to the first amplification stage for providing the regulated supply voltage.

66. A power amplifier circuit according to claim 65, wherein the voltage regulator circuit comprises an operational amplifier circuit, the operational amplifier circuit having a first input port, a second input port and an output port, the first input port thereof coupled to the control port for receiving the control signal and the output port thereof coupled to a gate terminal of the FET.

67. A power amplifier circuit according to claim 66, comprising a regulated voltage sense circuit disposed between one of the drain and source terminals of the FET and the

second input port of the operational amplifier circuit, the regulated voltage sense circuit for sampling the regulated supply voltage from the FET.

68. A power amplifier circuit according to claim 67, wherein the regulated voltage sense circuit comprises a voltage divider circuit.

69. A power amplifier circuit according to claim 67, wherein the regulated voltage sense circuit comprises an amplitude shifting circuit.

70. A power amplifier circuit according to claim 62, wherein each amplification stage comprises at least a transistor having an emitter terminal, a collector terminal and a base terminal, one of the emitter and collector terminals coupled to one of the supply voltage and regulated supply voltage and the other one of the emitter and collector terminals coupled to ground.

71. A power amplifier circuit according to claim 70, wherein each amplification stage comprises at least a current source coupled to the base terminal of the at least a transistor.

72. A power amplifier circuit according to claim 71, wherein the at least a current source is integrated on a same die as the power amplifier circuit.

73. A power amplifier circuit according to claim 62, wherein each amplification stage comprises at least a transistor having a drain terminal, a source terminal and a gate terminal, one of the source and drain terminals coupled to one of the supply voltage and regulated supply voltage and the other one of the source and drain terminals coupled to ground.

74. A power amplifier circuit according to claim 73, wherein each amplification stage comprises at least a voltage source coupled to the gate terminal of the at least a transistor.

75. A power amplifier circuit according to claim 74, wherein the at least a voltage source is integrated on a same die as the power amplifier circuit.